- - REMARKS - -

The present amendment replies to a Final Office Action dated December 2, 2002. Claims 1-10 are currently pending in the present application. The Applicant has amended independent claim 1 herein to obviate a rejection of independent claim 1.

In the Final Office Action, Examiner Brown rejected pending claims 1-10 under 35 under 35 U.S.C. §103(a) as being unpatentable over Dallas Semiconductor *DC87C550 Data Sheet* in view of U.S. Patent No. 5,416,769 to *Pawloski*. The Applicant has thoroughly considered Examiner Baker's remarks concerning the §103(a) rejection of independent claims 1 and 10, and again carefully reviewed the *DC87C550 Data Sheet* and the *Pawloski* in combination. The Applicant respectfully traverses this §103(a) rejection of independent claims 1 and 10 as subsequently recited herein, and respectfully requests reconsideration of the present application.

As to the traversal, the Applicant respectfully concurs with Examiner Baker that the *DC87C550 Data Sheet* discloses a data processing device comprising "a register circuit for storing at least two addresses in parallel" as recited in independent claims 1 and 10. The Applicant also respectfully concurs with Examiner Baker that *DC87C550 Data Sheet* fails to disclose, teach or suggest the data processing device comprising "a control register that is instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction" as recited in independent claim 1 and "a control register in communication with said register selector register and said logic circuit, said control register being instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction" as recited in independent claim 10.

In opposition to Examiner Brown, the Applicant respectfully asserts that the modification of the data processing device of the *DC87C550 Data Sheet* to incorporate the auto-increment/auto decrement control SFR illustrated in FIG. 8 of *Pawloski* as proposed by Examiner Brown would render the data processing device of the *DC87C550 Data Sheet* unsatisfactory for its intended purpose. Specifically, the control SFR of

Pawloski as illustrated in FIG. 8 is employed to enable/disable incrementing operations and decrementing operations of a single address_SFR of page0, a single address_SFR of page1, a single address_ SFR of page2, and a single address_SFR of page3. *Pawloski* however fails to teach or suggest the outputs of two or more of single address-SFRs being connected in parallel to provide a single address to one of the pages0-3. Second, *Pawloski* fails to teach or suggest one or more of the pages0-3 including two or more address-SFRs having their outputs connected in parallel to provide a single address to the corresponding page.

Pawloski therefore clearly fails to provide an enabling description of the control SFR as being capable of controlling two or more address-SFRs having their outputs connected in parallel to provide a single address to one of the pages0-3. Thus, in order to incorporate the auto-increment/auto decrement control SFR illustrated in FIG. 8 of *Pawloski* into the data processing device of the *DC87C550 Data Sheet* as proposed by Examiner Brown, the data processing device of the *DC87C550 Data Sheet* would have to be modified to comprise a register circuit for storing at least two addresses that are not in parallel. This of course would render the data processing device of the *DC87C550 Data Sheet* unsatisfactory for its intended purpose, and consequently, there is no suggestion or motivation to make the proposed modification of the data processing device of the *DC87C550 Data Sheet* to incorporate the auto-increment/auto decrement control SFR of *Pawloski*.

Withdrawal of the rejection of independent claims 1 and 10 under 35 U.S.C. §103(a) as being unpatentable over *DC87C550 Data Sheet* in view of *Pawloski* is therefore respectfully requested.

Claims 2-9 depend from independent claim 1. Therefore, dependent claims 2-9 include all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claims 2-9 are allowable over *Roux* for at least the same reason as set forth with respect to independent claim 1. Withdrawal of the rejection of dependent claims 2-9 under 35 U.S.C. §103(a) as being

unpatentable over *DC87C550 Data Sheet* in view of *Pawloski* is therefore respectfully requested.

SUMMARY

Examiner Baker's objection to claim 1 has been obviated by amendment herein to independent clam 1. Examiner Baker's 35 U.S.C. §103(a) rejection of claims 1-10 have been obviated by the above remarks concerning the patentability of independent claims 1-10 over *DC87C550 Data Sheet* in view of *Pawloski*. The Applicant respectfully submits that claims 1-10 fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested.

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Respectfully submitted,
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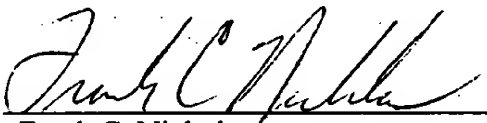

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Twice Amended) A data processing device, comprising

a register circuit for storing at least two addresses in parallel;

an address selector [including a register selector register and a logic circuit collectively] arranged to cycle through a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states; and

a control register [in communication with said register selector register and said logic circuit, said control register] that is instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction.